

Applicant : Chinnugounder Senthilkumar et al.  
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REMARKS

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold type.

**Claim 21 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Martin et al. 4,977,380 (Martin).**

Figures 4, 5a and 5b in combination with the entire disclosure of Martin disclose an apparatus for providing a variable level of capacitance having a plurality of capacitors (C 13, C14 ... ), each selectable through an independent control signal (In Figures 4 and 5b of Martin, note the signal lines individually connected to the gates of the switching elements like Q14 that control which capacitor is connected in or out of the circuit.) These independent control signals are generated by a logic circuit (Note Figure 5a that clearly shows logic elements like U6A, U6B that forms a logic circuit.) The selected capacitors of Martin clearly provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors. Martin also clearly discloses buffer circuitry (Note Figure 5b that shows the use of buffer circuitry like U9E. Also note column 4, around line 21 that describes these elements as "buffers".) These buffers inherently isolate. Thus in the circuit of Martin these buffers decouple the plurality of capacitors from the logic circuit that clearly prevents noise in the logic circuit from affecting the plurality of capacitors.

Martin does not disclose or suggest "MOSFET capacitors, each capacitor selectable by an independent control signal generated by a logic circuit, the selected capacitors to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors," as recited in amended claim 21.

While Martin discloses "a switched bank of capacitors C3 through C15" (col. 2:57-58), Martin does not disclose or suggest that the capacitors be MOSFET capacitors. It would not have been obvious to use MOSFET capacitors for the capacitors C3 to C15 in Martin because, the capacitances of the MOSFET capacitors are subject to variations with changes in the power supply voltage, and there may be leakage current from source or drain nodes to the body of the

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MOSFET, causing the capacitances to change. The applicant was the first to recognize that these issues could be alleviated to enable MOSFET capacitors to be selected to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors.

Claims 22 and 23 are patentable for at least the same reasons as claim 21.

Any circumstance that the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges to deposit account 06-1050, referencing attorney docket 10559-650003.

Respectfully submitted,

Date: 7/7/2004

  
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\* See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 10.9(b).

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